Volume 3, Issue 1 (2015) 275-279 ISSN 2347 - 3258
International Journal of Advance Research and Innovation

FPGA Based PWM of Cascaded Multilevel Voltage Source Inverter

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Article Info
Article history:
Received 10 February 2015
Received in revised form
15 February 2015
Accepted 28 February 2015
Available online 15 March 2015

Keywords
Cascaded H-Bridge multilevel Inverter,
Digital Pulse Width Modulation (DPWM),
FPGA

Abstract
Multilevel inverters have grasped attention in the past few years as power converters in many applications. They are advantageous over the conventional two-level inverters because of the capability of reducing the lower order harmonic contents by increasing the number of levels. Many studies and research have been done for generation of modulating signals for multilevel inverters. Modulation signal generation methods for these inverters include staircase modulation, sine-triangle carrier modulation, space vector modulation etc. Various topologies of multilevel inverter provides several advantages including lower voltage stress, higher efficiency, lower EMI, better waveform and improved THD. This paper presents the development of Altium FPGA as a control circuit for generation of the digital pulse width modulation (DPWM) signal for the single-phase cascaded H-bridge multilevel inverter. The FPGA chip is chosen for the hardware implementation due to its ability to produce accurate results at a high computational speed. Counter based digital pulse width modulation (DPWM) for increased resolution without unnecessarily increasing the clock frequency is used. In addition to Altium Nanoboard FPGA, Xilinx System Generator/MATLAB software has been used for simulation and verification of the proposed circuit before implementation. The simulation and experimental results are in close agreement.

1. Introduction

Multilevel inverter finds its application in high voltage and high power converters, Large electric drives and utility applications require advanced power electronics converter to meet the high power demands. As a result, multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations. A multilevel converter not only achieves high power ratings, but also improves the performance of the whole system in terms of harmonics, dv/dt stresses, and stresses in the bearings of a motor. Several multilevel converter topologies have been developed; i) diode clamped, ii) flying capacitors, and iii) cascaded or H-bridge.

Referring to the literature reviews, the cascaded multilevel inverter (CMI) with separated DC sources is clearly the most feasible topology for use as a power converter for medium & high power applications due to their modularization and extensibility. The H-bridge inverter eliminates the excessively large number of

(i) Bulky transformers required by conventional multilevel inverters,
(ii) Clamping diodes required by multilevel diode-clamped inverters,
(iii) Flying capacitors required by multilevel flying-capacitor inverter.

The various topological structures of the multilevel inverter suggestions must cope with the following points:

1) Less number of switching devices,
2) Capable of enduring high voltage and high power,
3) Lower switching frequency for the switching devices, [1-3].

Digital pulse width modulation technique

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Cascaded H-bridge multilevel inverter is gaining faster development due to its topological and modularity significance.

Digital PWM generation is considered as an alternate modulation technique in place of the conventional sinusoidal PWM using triangular carriers for the multilevel inverter operation that has the advantages of implementation simplicity and possibility to reduce harmonic distortions. Some methods use carrier disposition and others use phase shifting of the multiple carrier signals.

Digital controllers, such as microprocessors, DSP, FPGA and application specific integrated circuits (ASIC) are gaining importance in the power electronics applications as they can easily implement DPWM, with better performance and at low cost [4-8]. Therefore, digital control techniques are becoming more common solutions in modem power converters .

Field Programmable Gate Array (FPGA)

The field programmable gate array (FPGA) circuits have become popular in the applications where high performance, low development, low production cost and fast time-to market are required. In fact, FPGA are functionally similar to standard asics but appear cost effective even in small-medium volume productions, thus allowing, the realization of powerful and cheap systems. Additionally, they almost eliminate the code portability issue as VHDL, the hardware description language, and several advanced development tools are almost device family independent.

One emerging field which can obtain significant advantages by the use of FPGA is the multilevel converters.

This is because the high number of switching components requires many output signals; needed to apply the modulation pattern to power devices. Most microcontrollers are not able to satisfy this demand. In fact, they can only generate few of them (generally six) because they are designed to control standard inverters. Multilevel converters often require complex control algorithms which cannot be implemented in real-time using standard low cost microcontrollers or DSP, but can be successfully implemented using hardware description languages and FPGA [9-11]. This paper presents a DPWM of multilevel inverter whose output voltage may have three or five levels based on modulation index. Xilinx ISE design suite14.2 is used to generate DPWM pattern and by the means Altium designer generated schematic diagrams and VHDL test bench programs the switching pattern is verified. The final design is converted in configuration data file and loaded into Altium nano board. Fig.1 shows the block diagram of cascade multilevel inverter with DPWM and FPGA

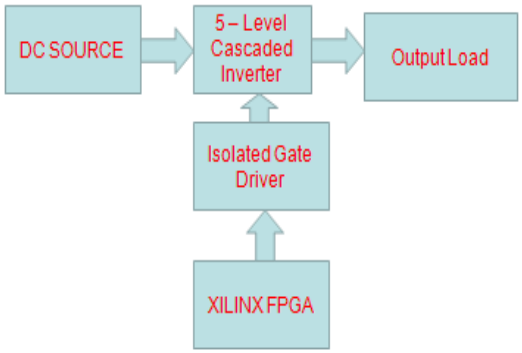

Fig: 1. Block Diagram of Cascade Multilevel Inverter

2. Cascaded Multilevel H-Bridge Inverter

C. Basic concept of multilevel inverter

Multilevel inverters are significantly different from the ordinary inverter where only two levels are generated. The semiconductor devices are not connected in series to for one single high-voltage switch. In which each group of devices contribute to a step in the output voltage waveform. The steps are increased to obtain an almost sinusoidal waveform. The number of switches involved is increased for every level increment.

The cascaded H-bridge multilevel inverter circuit is shown in Fig. 2. The number of H-bridges required for an n-level inverter are N = (n-1)/2. Single-phase structure of the five-level cascaded H-bridge inverter is shown in Fig. 2. The output phase voltage is equal to the summation of the output of the each H-bridge module as below.

$$V_{ac} = V_{dc/2} + V_{dc/2} + \ldots\ldots + V_{mh} \quad (1)$$

Where h is the number of H-bridge modules used in the multilevel circuit. Each module of the H-bridge has its own input voltage and consists of four switching power devices; S_a, S_b, S_c, and S_d. Each module of the cascaded multilevel inverter can produce three levels of the output voltage which is +V, 0 and -V. This is made possible by connecting the DC sources sequentially to the AC side via four power devices. For example cascaded

H-bridge multilevel inverter with four modules of the H-bridge will produce nine levels of the output phase voltage;

(4V, 3V, 2V, V, 0,-V,-2V,-3V and -4V).

The cascaded H-bridge multilevel inverter has several advantages because of its simple and modular circuit configuration. Each of its modules is identical and incorporates both input and output circuitry. Besides, the cascaded H-bridge multilevel inverter requires the least number of components compared to other types of multilevel inverter. These features provide flexibility in extending cascaded H-bridge multilevel inverter to higher number of levels without modification on the circuit itself.[23-25] The switching signal and the output voltage are shown in Table I.

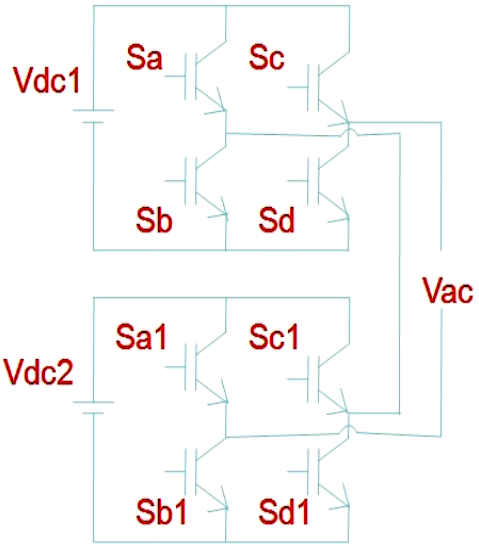

Fig: 2. The cascaded H-bridge multilevel inverter circuit

Table: 1. Gate Switching Signal for Cascaded Multilevel Inverter

Sa1	Sb1	Sc1	Sd1	Sa	Sb	Sc	Sd	Vac
0	1	1	0	1	0	0	1	Vdc
0	1	1	0	1	0	1	0	Vdc/2
0	0	0	0	0	0	0	0	0
1	0	0	1	1	0	1	0	-Vdc/2
1	0	0	1	0	1	1	0	-Vdc

3. FPGA Based Control Algorithm

The architecture of the FPGA consists of three types of configurable elements- a perimeter of input/output blocks (IOBs), a core array of configurable logic blocks (CLBs), and resources for interconnection. The IOBs provide a programmable interface between the internal array of logic blocks (CLBs) and the device's external package pins. CLBs perform user-specified logic functions, and the interconnect resources carry signals among the blocks. A

configuration program stored in internal static memory cells determines the logic functions and the interconnections [12-13].

The block diagram shown in fig. 3, represents the gating signal generated using dpwm for the cascaded h-bridge multilevel inverter as shown in the fig. 3, The technique uses comparison of different carrier signals with the SINUSOIDAL signal. The saw tooth waves as a carrier signals are used and generated by up counter devices in Xilinx system generator toolbox of the matlab. The first counter starts from 0 v to 1.0 v of saw tooth wave carrier signal, and second counter starts from 1.0 V to 2.0 V of the saw tooth wave carrier signal.

Similarly, each saw tooth wave carrier signal amplitude is kept with a constant amplitude and frequency of 1 kHz. The reference sinusoidal wave signal of 30 V amplitude and 50 Hz frequency is approximated by a stepped sinusoid generated using 5-bit up-counter with 14-bit memory (ROM) devices. The compared output signals are fed to the three-input XOR gates as shown in fig. 4, The unit of NOT gates deals with the four main signals produced from the comparators and the other four signals are obtained from the XOR gate directly as indicated by the switches S_a; S_b, S_c, S_d, S_{a1}, S_{b1} S_{c1}, S_{d1}. Here S_a, S_b, S_c, S_d signals are driving the conventional multilevel inverter (see figure 3) and S_a, S_b, S_c, S_d, S_{a1}, S_{b1} S_{c1}, S_{d1} signals are drivers for the cascaded multilevel inverter. The modulation index is defined as:

$$M = Vm / 2\,Vc \qquad (2)$$

Where V_m is the peak value of digital sinusoidal wave and V_c is the carrier peak value [12].

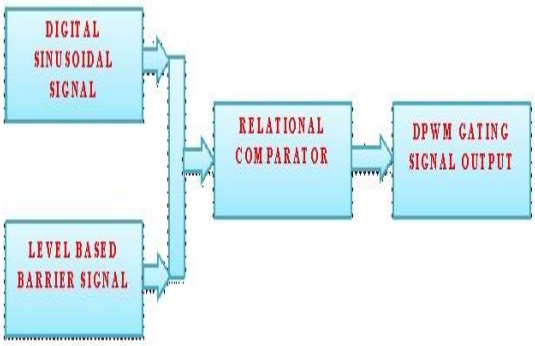

Fig: 3. Model for PWM Signals Generation

The corresponding VHDL program code is generated using the system generator after verification and simulation of the design. The VHDL program is verified and simulated using Xilinx-ISE 14.2 software [13-19].

The FPGA design flow comprises of the following steps:

1. System Requirement - it should assign constraints such as signal timing, pin allocation, and area constraints,
2. Circuit Design and synthesis- it is analyzed using Xilinx- block set Library.
3. Design implementation- implementation of the controller design, which includes the Translate, Map, Place and Route.
4. Complete Co-simulation- actual output is analyzed on MATLAB/Simulink and Xilinx System generator.
5. Testing and verification- includes both functional verification (also known as RTL simulation) and timing Verification. If it fails at any stage then again the analysis is done at designing stage.
6. Code Generation- in this HDL Netlist, NGC, Timing and power analysis is done and BIT file is generated.
7. Implementation and Code Downloading- program debugging or to download the target device of XILINX/SPARTAN-3E processor kit, to program the device with a programming cable (JTAG). [20-22] Once the program is dumped on the FPGA kit, it acts as a controller and generates gating pulses.

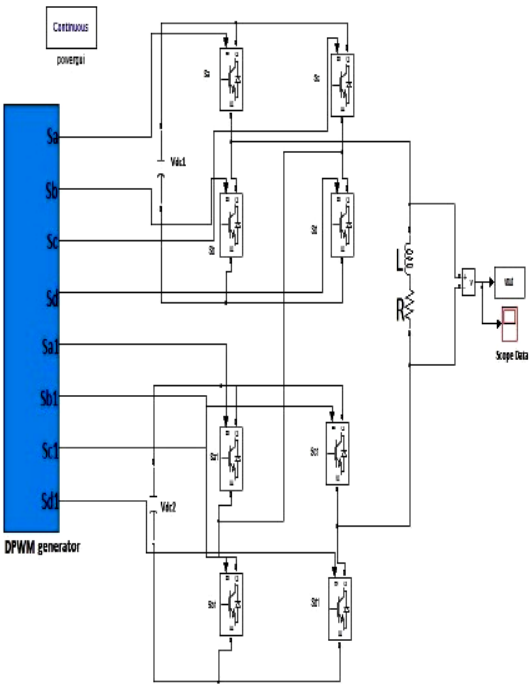

Fig: 4. System generator model of cascaded multilevel inverter

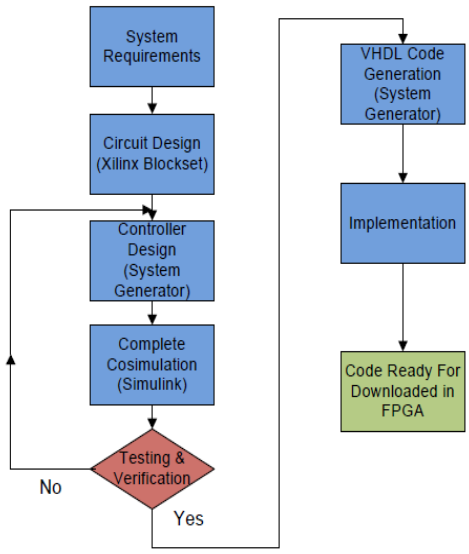

Fig: 5. Design flow diagram for MATLAB/Simulink and Xilinx System Generator

The output of the gating signal can be observed in digital storage oscilloscope (DSO). Fig. 4 shows the flow chart of the FPGA design embedded in a single chip for generating gate signals to drive the single-phase cascaded multilevel inverter. The output across each header is connected to the header generated fromthe Schematic of the Altium Designer and is connected through the driver to each switching devices of the PWM single phase inverter.

4. Results

The proposed five-level cascaded multilevel PWM single phase inverter is simulated by using MATLAB/Simulink®, The system is tested and simulated with resistive and inductive loads. The circuit diagram of pulse generator is shown in the fig. 5, The five different levels of the carrier signals (such as square wave signals) are compared with the sinusoidal (reference signal) as shown in fig. 6, The 30 V amplitude and 50 Hz frequency sine wave is produced by up-counter along with ROM devices. The output voltage waveform of five-level cascaded H-bridge inverter has been simulated and shown in fig. 7, Eight DPWM gating signals for firing the cascaded h-bridge inverter across the scope is shown in Fig. 8.

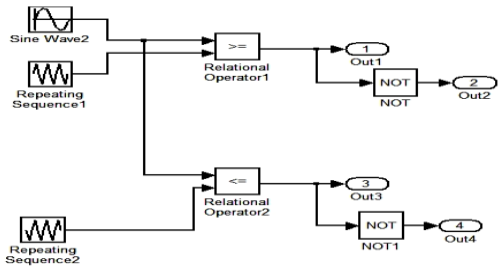

Fig: 6. Circuit Diagram of Pulse Generator

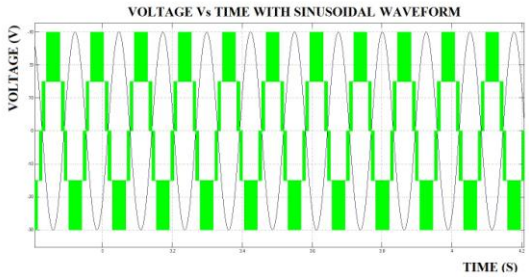

Fig: 7. Carrier Signals Compared with Sinusoidal Signals

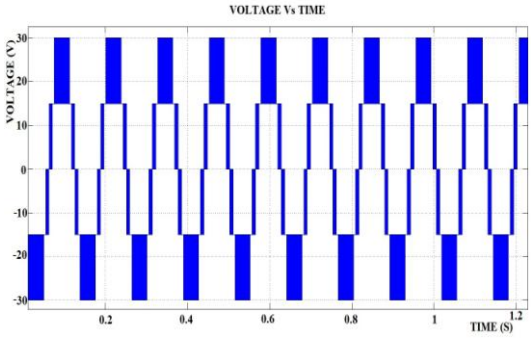

Fig: 7. Five-Level Cascade Multilevel Inverter Output Waveform

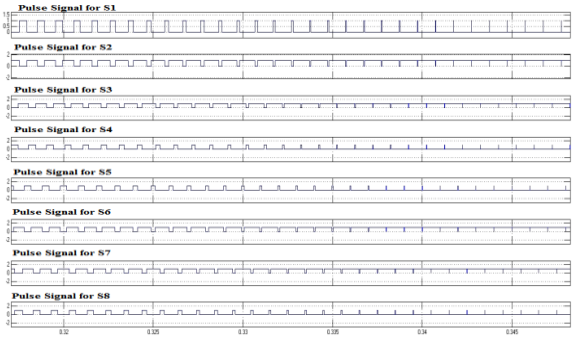

Fig: 9. Eight gating signals for firing the cascade H-bridge Inverter

The VHDL schematic entity is developed for DPWM generation using Altium designer board and the result is displayed on digital storage oscilloscope. The six different levels of the carrier signals (such as saw tooth signals) are compared with the sinusoidal (reference signal) as shown in fig. 9, Each saw tooth signal is of the same amplitude and same frequency of 1 kHz that is generated from the up-counter. The 30 V amplitude and 50 Hz frequency sine wave is produced by up-counter along with ROM devices.

The proposed inverter is simulated and desired output waveforms are presented, thus the five-level output waveforms are achieved and gating pulses are generated to provide gate pulse to the switches of cascade H-bridge multilevel inverter. The gating circuit in which provides the required pulses are as shown in the fig. 5, these five level output waveforms are achieved by proper gate pulses.

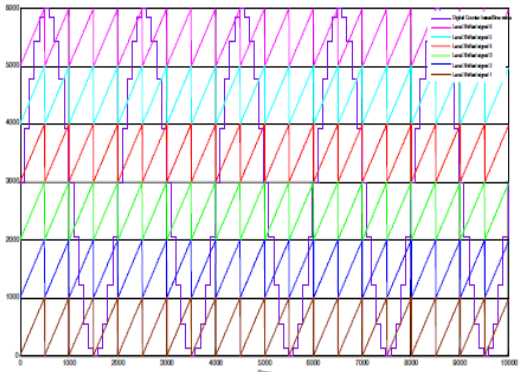

Fig: 9. Six Different Levels of Saw Tooth Carrier Signal Compared with Digital Sinusoidal Counter Based Signal

5. Conclusion

The Altium based FPGA digital control switching patterns are adopted and applied to the cascaded multilevel inverter switches to generate multilevel output voltages. The FPGA reduces complexity, increases speed and adds flexible in the design of the control circuit for hardware implementation. It can efficiently extend the range of modulation index which facilitates a better quality output voltage with minimal distortion. The experimental, simulation and hardware implementation results demonstrate the improved quality voltage waveform shapes at the output of the inverter.

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